Industrial eMMC

FBGA153 Datasheet

V1.00

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1 Introduction

1.1 General Description

eMMC is an embedded storage solution designed in a PBGA package form. The operation of eMMC is a simple read and write to memory using eMMC protocol v5.1 which is an industry standard.

The eMMC consists of NAND flash and a MMC controller. 3.3V supply voltage is required for the NAND area (V_{CC}), whereas 1.8V or 3.3V dual supply voltage (V_{CC} or V_{CCQ}) is supported for MMC controller.

eMMC has high performance at a competitive-cost, high quality and low power consumption to meet customer extremely demanding application scenario.

1.2 Product List

Table1: Product Information(DYExxxGFTI-EX)

Part Number	Density	Package size[1]	Package Type	Thickness Type
DYE008GFTI-EX	8GB	11.50×13.00×1.00(mm)	PBGA-153-Ball	1
DYE016GFTI-EX	16GB	11.50×13.00×1.00(mm)	PBGA-153-Ball	1
DYE032GFTI-EX	32GB	11.50×13.00×1.00(mm)	PBGA-153-Ball	1
DYE064GFTI-EX	64GB	11.50×13.00×1.00(mm)	PBGA-153-Ball	1
DYE128GFTI-EX	128GB	11.50×13.00×1.00(mm)	PBGA-153-Ball	1
DYE256GFTI-EX	256GB	11.50×13.00×1.00(mm)	PBGA-153-Ball	1

Note :

1: The thickness is the maximum value in the size. Please refer to the package size diagram for the actual size.

1.3 Key Feature

- **eMMC V5.1 compatible. Detail description is referenced by JEDEC Standard**

- (Backward compatible to eMMC V4.5 to V5.0)

- **Bus mode**

- Data bus width: 1 bit (default), 4 bit and 8 bit

- Data transfer rate: up to 400MB/s(HS400)@ 200MHz DDR with 8bit bus width

- MMC I/F Clock Frequency: 0~200MHz
- MMC I/F Boot Frequency: 0~52MHz

■ **Operating Voltage Range**

- V_{CC}(NAND)：3.3V
- V_{CCQ}(Controller)：3.3V/1.8V

■ **Temperature**

- Operation：
- DYExxxGFTI-EX: -40℃~85℃
- Storage without operation：
- DYExxxGFTI-EX: -50℃~90℃

■ **Humidity level**

- MSL-3

■ **Weight**

- 0.4±0.1g

■ **Absolute maximum rating**

- V_{CC}：-0.5V~4.1V
- V_{CCQ}：-0.5V~4.1V

■ **Supports Features.**

- HS400，HS200，DDR52，SDR52
- High Priority Interrupt (HPI)
- Background Operation, **BKOPS Control**
- Packed CMD，**Command Queuing**
- Cache，**Cache Flushing Report**，**Cache Barrier**(Optional)

- Partitioning, Partition types, RPMB，**RPMB Throughput Improve**
- Discard，Trim，Erase，Sanitize
- Write Protect, **Secure Write Protection** (Optional)
- Lock/Unlock
- Power Off Notification (PON), Sleep/Awake
- Enhance Reliable Write
- Boot feature，Boot partition
- HW/SW Reset
- Configurable driver strength

■ Guarantee period

- 1 year

2 Package Configuration

2.1 The ball array view

DYExxxGFTI-EX top view is shown in figure 1, functional pin description is shown in table 2.

Figure1: Top view(153 Ball Side down View)

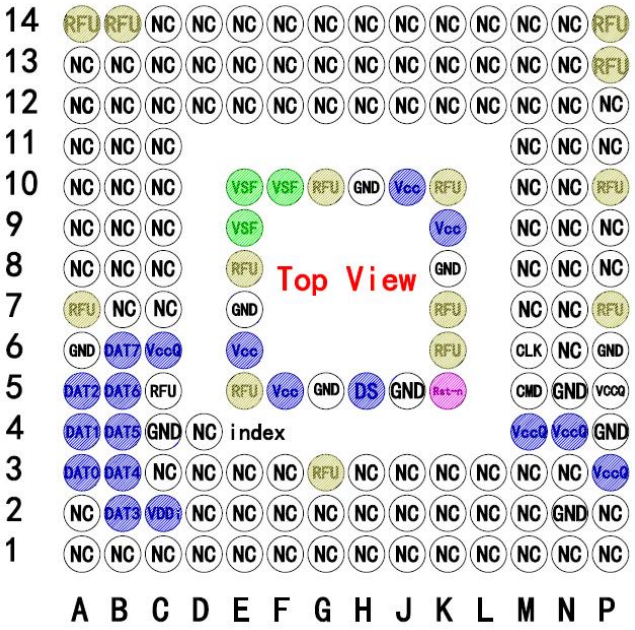


Table2: Functional pin (153 ball)

Ball No.	Name	Ball No.	Name	Ball No.	Name	Ball No.	Name
A3	DAT0	H5	DS	P3	V_{CCQ}	H10	V_{SS}
A4	DAT1	K5	RST_n	P5	V_{CCQ}	J5	V_{SS}
A5	DAT2	C2	VDDi	C4	V_{SSQ}	K8	V_{SS}
B2	DAT3	E6	V_{CC}	N2	V_{SSQ}		
B3	DAT4	F5	V_{CC}	N5	V_{SSQ}		
B4	DAT5	J10	V_{CC}	P4	V_{SSQ}		
B5	DAT6	K9	V_{CC}	P6	V_{SSQ}		
B6	DAT7	C6	V_{CCQ}	A6	V_{SS}		
M6	CLK	M4	V_{CCQ}	E7	V_{SS}		
M5	CMD	N4	V_{CCQ}	G5	V_{SS}		

Functional pin for description see 2.2 Ball Assignment.
NC: No Connect, can be connected to ground or left floating.
RFU: Reserved for Future Use, should be left floating for future use.
VSF: Vendor Specific Function, shall be left floating.

2.2 Ball Assignment

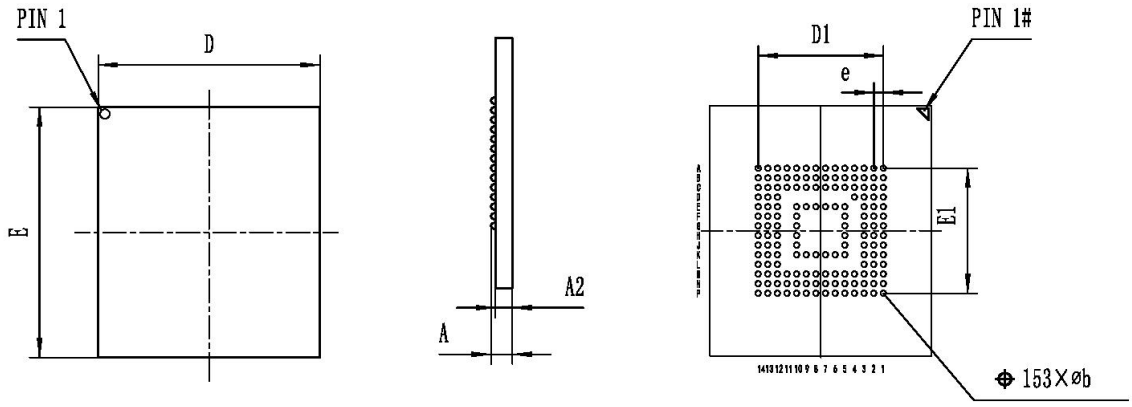
Table3: Ball Assignment

Signal	Ball No.(BGA153)	Ball No.(BGA100)	Type	Description
CLK	M6	P6	I	Each cycle of the clock directs a transfer on the command line and on the data lines.
CMD	M5	P5	I/O	This signal is a bidirectional command channel used for device initialization and command transfer. The CMD Signal has 2 operation modes: open drain for initialization, and push-pull for fast command transfer.
DATA(DAT 0-DAT7)	A3，A4，A5，B2，B3，B4，B5，B6	K2，N2，K3，N3，N8，K8，N9，K9	I/O	These are bidirectional data channels. The DAT signals operate in push-pull mode.
RST_n	K5	M5	I	Hardware Reset Input
DS	H5	K5	O	Data Strobe: Return Clock signal used in HS400 mode
V_{CCQ}	C6，M4，N4，P3，P5	L2，L4，L7，L9，P3，P8，H3，H8	P	Power supply for MMC interface and Controller, have two power mode: High power mode:3.3V; Lower power mode:1.8V
V_{CC}	E6，F5，J10，K9	F2，F3，F4，F5，F6，F7，F8，F9	P	Power supply for NAND flash memory, its power voltage range is: 3.3V.
VDDi	C2	E4	P/O	VDDi is internal power mode. Connect 0.1uF or 2.2uF capacitor from VDDi to ground
V_{SSQ}，V_{SS}	A6，E7，G5，H10，J5，K8，C4，N2，N5，P4，P6	G2，G3，G4，G5，G6，G7，G8，G9，H2，H9，J5，L3，L8，M4，M7，P2，P9	G	Ground lines

I : input
O: output
I/O: bidirectional
P: power
G: ground
P/O: power output, without power supply

2.3 Package Dimensions

Figure2: Package Dimensions(153 ball)



Note: material of lead-free solder ball is SAC305.

Table4: Thickness Type 1

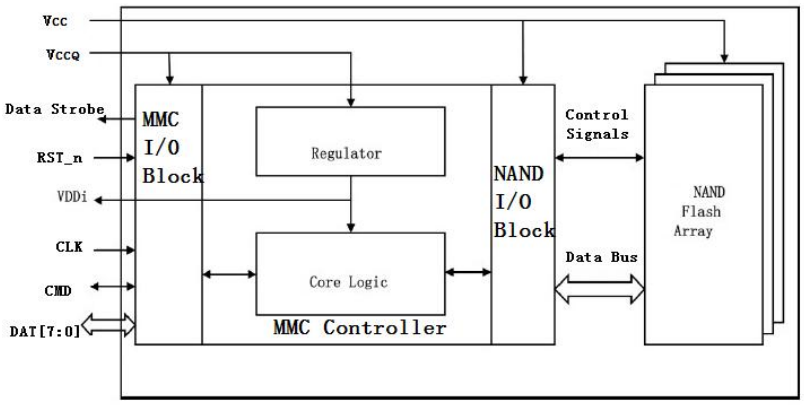
Unit: mm

Name	Min	Type	Min	Name	Min	Type	Min
A2	0.58	0.68	0.78	E1	6.45	6.50	6.55
A	0.80	0.90	1.00	D1	6.45	6.50	6.55
E	12.90	13.00	13.10	e	0.48	0.50	0.52
D	11.40	11.50	11.60	b	0.25	0.30	0.35

2.4 Product architecture

eMMC consists of MMC controller and NAND FLASH, MMC controller through NAND IO interface connected to the NAND FLASH IO, and be responsible for management of NAND FLASH as eMMC IO interface for foreign, mainly to complete the interface protocol parsing. eMMC internally integrated LDO, through the V_{CCQ} is converted to a MMC controller core logic of power supply.

Figure3: eMMC architecture



3 Basic feature

3.1 User Density Size

Table5: User Density Size

Capacity	User Area Capacity	SEC_COUNT in Extended CSD
8GB	7456MB	0x00E90000
16GB	14910MB	0x01D1F000
32GB	29820MB	0x03A3E000
64GB	59640MB	0x0747C000
128GB	119280MB	0x0E8F8000
256GB	238560MB	0x1D1F0000

3.2 Power consumption

Reading and writing power consumption:

Table6: Read/write power

Capacity	Mode	Read (mA)		Write (mA)	
		ICC	ICCQ	ICC	ICCQ
8GB	HS400	132	109	135	109
16GB	HS400	137	116	137	112
32GB	HS400	145	124	141	120
64GB	HS400	150	145	142	122
128GB	HS400	165	155	143	124
256GB	HS400	176	155	145	125

Test conditions: At 25 ℃, V_{CC} = 3.3V, V_{CCQ} = 1.8V, oscilloscope test average current in the corresponding power supply of 100ms.

Idle power consumption:

Table7: Idle power

Capacity	Mode	Standby（mA）		Dormant（mA）	
		ICC	ICCQ	ICC	ICCQ
8GB	/	0.08	2.6	0	2.7
16GB	/	0.085	2.7	0	2.9

32GB	/	0.085	3.1	0	3.2
64GB	/	0.1	3.2	0	3.2
128GB	/	0.11	3.3	0	3.2
256GB	/	0.11	3.3	0	3.3

Test conditions: At 25℃, V_{CC} = 3.3V, V_{CCQ} = 1.8V test.

3.3 Performance

Table8: Performance (DYExxxGFTI-EX)

Capacity	Mode	Performance			
		Sequential write (MB/s)	Sequential read (MB/s)	Random Write(IOPS)	Random read (IOPS)
8GB	HS400	Up to 120	Up to 220	Up to 2800	Up to 3100
16GB	HS400	Up to 120	Up to 240	Up to 2800	Up to 3200
32GB	HS400	Up to 120	Up to 260	Up to 3000	Up to 3300
64GB	HS400	Up to 200	Up to 260	Up to 3000	Up to 3600
128GB	HS400	Up to 200	Up to 260	Up to 3100	Up to 3700
256GB	HS400	Up to 210	Up to 260	Up to 3200	Up to 3800

Test condition: GL3227e card reader, USB 3.0, FAT32 file system, empty state.

3.4 Working mode

Table9: Working mode

Device Type	Clock frequency	Power supply	Bus width (bit)
HS400 Mode	0-200MHz DDR	V_{CC}=3.3V，V_{CCQ}=1.8V	8
HS200 Mode	0-200MHz SDR	V_{CC}=3.3V，V_{CCQ}=1.8V	4、8
HS Mode	0-52MHz DDR	V_{CC}=3.3V，V_{CCQ}=3.3/1.8V	4、8
	0-52MHz SDR	V_{CC}=3.3V，V_{CCQ}=3.3/1.8V	1、4、8
Compatibility Mode	0-26MHz SDR	V_{CC}=3.3V，V_{CCQ}=3.3/1.8V	1、4、8

4 Device Register

4.1 CID register

The Device IDentification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (eMMC protocol). Every individual flash or I/O Device shall have a unique identification number. Every type of eMMC Device shall have a unique identification number. Table 75 lists these identifiers. The structure of the CID register is defined in this section.

Table10: CID register Field Parameters

CID bits	Field	Name	width	Default
[127:120]	MID	Manufacturer ID	8	0xBA
[119:114]	-	Reserved	6	0
[113:112]	CBX	Card/BGA	2	0x1
[111:104]	OID	OEM/application ID	8	0x59
[103:56]	PNM	Product name	48	0x44 59 45 46 54 49 （DYEFTI）
[55:48]	PRV	Product revision	8	0x10
[47:16]	PSN	Product serial number	32	-
[15:8]	MDT	Manufacturing date	8	-
[7:1]	CRC	CRC7 checksum	7	-
[0]	-	Not used; always 1	1	0x1

Customers if have any special needs, please contact manufacturer to customize CID register contents.

4.2 OCR register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices.

Table11: OCR register

OCR bits	V_{CCQ} voltage range	Name	Width	Value(Note)
[6:0]	-	Reserved	7	000 0000b
[7]	1.7V~1.95V	Low level mode	1	1b
[14:8]	2.0V~2.6V	Medium level mode	7	000 0000b
[23:15]	2.7V~3.6V	High level mode	9	1 1111 1111b

OCR bits	V_{CCQ} voltage range	Name	Width	Value(Note)
[28:24]	-	Reserved	5	0 0000b
[30:29]	Access Mode	Access mode	2	10b(sector mode)
[31]	status bit	Device statusbit	1	Busy(0)/ready(1)

4.3 CSD register

The Card-Specific Data register provides information on how to access the eMMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:

R: Read only

W: One time programmable and not readable.

R/W: One time programmable and readable.

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Table12: CSD register

CSD bits	Field	Name	Cell type	Width	CSD value
[127:126]	CSD_STRUCTURE	CSD structure	R	2	0x3
[125:122]	SPEC_VERS	System specification version	R	4	0x4
[121:120]	-	Reserved	R	2	-
[119:112]	TAAC	Data read access time	R	8	0x2F
[111:104]	NSAC	Data read access time in CLK cycles (NSAC × 100)	R	8	0x1
[103:96]	TRAN_SPEED	Maximum bus clock frequency	R	8	0x2A
[95:84]	CCC	Card command classes	R	12	0x9F5
[83:80]	READ_BL_LEN	Maximum read data block	R	4	0x9

CSD bits	Field	Name	Cell type	Width	CSD value
		length			
[79:79]	READ_BL_PARTIAL	Partial blocks for reads supported	R	1	0x0
[78:78]	WRITE_BLK_MISALIGN	Write block misalignment	R	1	0x0
[77:77]	READ_BLK_MISALIGN	Read block misalignment	R	1	0x0
[76:76]	DSR_IMP	DS register implemented	R	1	0x0
[75:74]	-	Reserved	R	2	-
[73:62]	C_SIZE	Device size	R	12	0xFFF
[61:59]	VDD_R_CURR_MIN	Maximum read current at VDD, min	R	3	0x6
[58:56]	VDD_R_CURR_MAX	Maximum read current at VDD, max	R	3	0x6
[55:53]	VDD_W_CURR_MIN	Maximum write current at VDD, min	R	3	0x6
[52:50]	VDD_W_CURR_MAX	Maximum write current at VDD, max	R	3	0x6
[49:47]	C_SIZE_MULT	Device size multiplier	R	3	0x7
[46:42]	ERASE_GRP_SIZE	Erase group size	R	5	0x1F
[41:37]	ERASE_GRP_MULT	Erase group size multiplier	R	5	0x1F
[36:32]	WP_GRP_SIZE	Write protect group size	R	5	0x1F
[31:31]	WP_GRP_MULT	Write protect group enable	R	1	0x1
[30:29]	ECC DEFAULT_ECC	Manufacturer default ECC	R	2	0x0
[28:26]	R2W_FACTOR	Write-speed factor	R	3	0x1
[25:22]	WRITE_BL_LEN	Maximum write data block length	R	4	0x9
[21:21]	WRITE_BL_PARTIAL	Partial blocks for writes supported	R	1	0x0
[20:17]	-	Reserved	R	4	-
[16:16]	CONTENT_PROT_APP	Content protection application	R	1	0x0
[15:15]	FILE_FORMAT_GRP	File-format group	R/W	1	0x0
[14:14]	COPY	Copy flag (OTP)	R/W	1	0x0
[13:13]	PERM_WRITE_PROTECT	Permanent write protection	R/W	1	0x0
[12:12]	TMP_WRITE_PROTECT	Temporary write protection	R/W/E	1	0x0
[11:10]	FILE_FORMAT	File format	R/W	2	0x0
[9:8]	ECC	ECC	R/W/E	2	0x0
[7:1]	CRC	CRC	R/W/E	7	-
[0]	-		-	1	0x1

4.4 Extended CSD register

The Extended CSD register defines the eMMC properties and selected modes. It is 512 bytes long.

The most significant 320 bytes are the Properties segment, which defines the eMMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the

configuration the eMMC is working in. These modes can be changed by the host by means of the SWITCH command.

R: Read only

W: One time programmable and not readable.

R/W: One time programmable and readable.

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Table13: ECSD Register Field Parameters

ECSD Bytes	Field	Name	Cell Type1	Size (Bytes)	ECSD Value
[511:506]	-	Reserved	TBD	6	-
[505]	EXT_SECURITY_ERR	Extended Security Error	R	1	0x0
[504]	S_CMD_SET	Supported command sets	R	1	0x1
[503]	HPI_FEATURES	HPI features	R	1	0x3
[502]	BKOPS_SUPPORT	Background operations support	R	1	0x1
[501]	MAX_PACKED_READS	Max packed read command	R	1	0x3F
[500]	MAX_PACKED_WRITES	Max packed write command	R	1	0x3F
[499]	DATA_TAG_SUPPORT	Data tag support	R	1	0x1
[498]	TAG_UNIT_SIZE	Tag unit size	R	1	0x1
[497]	TAG_RES_SIZE	Tag Resource Size	R	1	0x0
[496]	CONTEXT_CAPABILITIES	Context management capabilities	R	1	0x5
[495]	LARGE_UNIT_SIZE_M1	Large unit size	R	1	0x0
[494]	EXT_SUPPORT	Extended partitions attribute support	R	1	0x3
[493]	SUPPORTED_MODES	Supported modes	R	1	0x1
[492]	FFU_FEATURES	FFU features	R	1	0x1

ECSD Bytes	Field	Name	Cell Type1	Size (Bytes)	ECSD Value
[491]	OPERATION_CODE_TIMEOUT	Operation codes timeout	R	1	0x17
[490:487]	FFU_ARG	FFU Argument	R	4	0x0
[486]	BARRIER_SUPPORT	Barrier support	R	1	0x0
[485:309]	-	Reserved	TBD	-	-
[308]	CMDQ_SUPPORT	CMDQ support	R	1	0x0
[307]	CMDQ_DEPTH	CMDQ depth	R	1	0x0
[306]	-	Reserved	TBD	1	-
[305:302]	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	Number of received sectors	R	4	0x0
[301:270]	VENDOR_PROPRIETARY_HEALTH_REPORT	Vendor proprietary health report	R	32	0x0
[269]	DEVICE_LIFE_TIME_EST_TYP_B	Device life time estimation type B	R	1	0x1
[268]	DEVICE_LIFE_TIME_EST_TYP_A	Device life time estimation type A	R	1	0x1
[267]	PRE_EOL_INFO	Pre EOL information	R	1	0x1
[266]	OPTIMAL_READ_SIZE	Optimal read size	R	1	0x8
[265]	OPTIMAL_WRITE_SIZE	Optimal write size	R	1	0x8
[264]	OPTIMAL_TRIM_UNIT_SIZE	Optimal trim unit size	R	1	0x8
[263:262]	DEVICE_VERSION	Device version	R	2	0x0
[261:254]	FIRMWARE_VERSION	Firmware version	R	8	-
[253]	PWR_CL_DDR_200_360	Power class for200MHz DDR at V_{CC}=3.6V	R	1	0x0
[252:249]	CACHE_SIZE	Cache size	R	4	0x100
[248]	GENERIC_CMD6_TIME	Generic CMD6 timeout	R	1	0x32
[247]	POWER_OFF_LONG_TIME	Power-off notification(long) timeout	R	1	0x3C
[246]	BKOPS_STATUS	Background operations status	R	1	0x0
[245:242]	CORRECTLY_PRG_SECTORS_NUM	Number of correctly programmed sectors	R	4	0x0
[241]	INI_TIMEOUT_AP	First Initialization time after partitioning	R	1	0x1E
[240]	CACHE_FLUSH_POLICY	Cache Flushing Policy	R	1	0x0
[239]	PWR_CL_DDR_52_360	Power class for 52MHz, DDR at 3.6V	R	1	0x0
[238]	PWR_CL_DDR_52_195	Power class for 52MHz, DDR at 1.95V	R	1	0x0
[237]	PWR_CL_200_195	Power class for 200MHz at V_{CCQ}=1.95V, V_{CC}=3.6V	R	1	0x0
[236]	PWR_CL_200_130	Power class for 200MHz at V_{CCQ}=1.3V, V_{CC}=3.6V	R	1	0x0
[235]	MIN_PERF_DDR_W_8_52	Minimum write performance for 8bit at	R	1	0x0

ECSD Bytes	Field	Name	Cell Type1	Size (Bytes)	ECSD Value
		52MHz in DDR mode			
[234]	MIN_PERF_DDR_R_8_52	Minimum read performance for 8bit at 52MHz in DDR mode	R	1	0x0
[233]	-	Reserved	TBD	1	-
[232]	TRIM_MULT	TRIM Multiplier	R	1	0x2
[231]	SEC_FEATURE_SUPPORT	Secure feature support	R	1	0x55
[230]	SEC_ERASE_MULT	Secure Erase Multiplier	R	1	0x1B
[229]	SEC_TRIM_MULT	Secure TRIM Multiplier	R	1	0x11
[228]	BOOT_INFO	Boot Information	R	1	0x7
[227]	-	Reserved	TBD	1	-
[226]	BOOT_SIZE_MULT	Boot partition size	R	1	0x20
[225]	ACC_SIZE	Access size	R	1	0x6
[224]	HC_ERASE_GRP_SIZE	High-capacity Erase unit size	R	1	0x1
[223]	ERASE_TIMEOUT_MULT	High-capacity Erase time out	R	1	0x1
[222]	REL_WR_SEC_C	Reliable write sector count	R	1	0x1
[221]	HC_WP_GRP_SIZE	High-capacity write protect group size	R	1	0x20
[220]	S_C_VCC	Sleep current V_{CC}	R	1	0x7
[219]	S_C_VCCQ	Sleep current V_{CCQ}	R	1	0x7
[218]	PRODUCTION_STATE_AWARENESS_TIMEOUT	Production state awareness timeout	R	1	0x17
[217]	S_A_TIMEOUT	Sleep/Awake time out	R	1	0x17
[216]	SLEEP_NOTIFICATION_TIME	Sleep Notification Time out	R	1	0x11
[215:212]	SEC_COUNT	Sector count	R	4	8GB: 0x00E90000 16GB: 0x01D1F000 32GB: 0x03A3E000 64GB: 0x0747C000 128GB: 0x0E8F8000 256GB: 0x1D1F0000
[211]	SECURE_WP_INFO	Secure Write Protection Mode	R	1	0x0
[210]	MIN_PERF_W_8_52	Minimum Write Performance for 8bit @52MHz	R	1	0x0
[209]	MIN_PERF_R_8_52	Minimum Read Performance for 8bit @52MHz	R	1	0x0
[208]	MIN_PERF_W_8_26_4_52	Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	R	1	0x0
[207]	MIN_PERF_R_8_26_4_52	Minimum Read Performance for 4bit @52MHz or 8bit	R	1	0x0

ECSD Bytes	Field	Name	Cell Type1	Size (Bytes)	ECSD Value
		@26MHz			
[206]	MIN_PERF_W_4_26	Minimum Write Performance for 4bit @26MHz	R	1	0x0
[205]	MIN_PERF_R_4_26	Minimum Read Performance for 4bit @26MHz	R	1	0x0
[204]	-	Reserved	TBD	1	-
[203]	PWR_CL_26_360	/	R	1	0x0
[202]	PWR_CL_52_360	/	R	1	0x0
[201]	PWR_CL_26_195	/	R	1	0x0
[200]	PWR_CL_52_195	/	R	1	0x0
[199]	PARTITION_SWITCH_TIME	Partition switching timing	R	1	0x5
[198]	OUT_OF_INTERRUPT_TIME	Out-of-interrupt busy timing	R	1	0x19
[197]	DRIVER_STRENGTH	I/O driver strength	R	1	0x1F
[196]	DEVICE_TYPE	Type of device	R	1	0x57
[195]	-	Reserved	TBD	1	-
[194]	CSD_STRUCTURE	CSD structure version	R	1	0x2
[193]	-	Reserved	TBD	1	-
[192]	EXT_CSD_REV	Extended CSD version	R	1	0x8
[191]	CMD_SET	Command Set	R/W/E_P	1	0x0
[190]	-	Reserved	TBD	1	-
[189]	CMD_SET_REV	Command set version	R	1	0x0
[188]	-	Reserved	TBD	1	-
[187]	POWER_CLASS	Power class	R/W/E_P	1	0x0
[186]	-	Reserved	TBD	1	-
[185]	HS_TIMING	High-speed interface timing	R/W/E_P	1	0x0
[184]	STROBE_SUPPORT	Strobe support	R	1	0x1
[183]	BUS_WIDTH	Bus width mode	W/E_P	1	0x0
[182]	-	Reserved	TBD	1	-
[181]	ERASE_MEM_CONT	Erased memory content	R	1	0x0
[180]	-	Reserved	TBD	1	-
[179]	PARTITION_CONFIG	Partition configuration	R/W/E&R /W/E_P	1	0x0
[178]	BOOT_CONFIG_PROT	Boot configuration protection	R/W&R/ W/C_P	1	0x0
[177]	BOOT_BUS_CONDITIONS	Boot bus conditions	R/W/E	1	0x0
[176]	-	Reserved	TBD	1	-
[175]	ERASE_GROUP_DEF	High-density erase group definition	R/W/E	1	0x0
[174]	BOOT_WP_STATUS	Boot write protection status register	R	1	0x0
[173]	BOOT_WP	Boot area write protection	R/W&R/	1	0x0

ECSD Bytes	Field	Name	Cell Type1	Size (Bytes)	ECSD Value
		register	W/C_P		
[172]	-	Reserved	TBD	1	-
[171]	USER_WP	User write protection register	R/W，R/W/C_P &R/W/E_P	1	0x0
[170]	-	Reserved	TBD	1	-
[169]	FW_CONFIG	Firmware configuration	R/W	1	0x0
[168]	RPMB_SIZE_MULT	RPMB size	R	1	0x20
[167]	WR_REL_SET	Write reliability setting register	R/W	1	0x0
[166]	WR_REL_PARAM	Write reliability parameter register	R	1	0x14
[165]	SANITIZE_START	Start Sanitize operation	W/E_P	1	0x0
[164]	BKOPS_START	Manually start background operations	W/E_P	1	0x0
[163]	BKOPS_EN	Enable background operations handshake	R/W& R/W/E	1	0x0
[162]	RST_n_FUNCTION	Hardware reset function	R/W	1	0x0
[161]	HPI_MGMT	HPI management	R/W/E_P	1	0x0
[160]	PARTITIONING_SUPPORT	Partitioning support	R	1	0x7
[159:157]	MAX_ENH_SIZE_MULT	Maximum enhanced area size	R	3	8GB: 0x0001D2 16GB: 0x00013B 32GB: 0x000264 64GB: 0x0004EC 128GB: 0x000993 256GB: 0x000930
[156]	PARTITIONS_ATTRIBUTE	Partitions attribute	R/W	1	0x0
[155]	PARTITION_SETTING_COMPLETED	Partitioning setting	R/W	1	0x0
[154:143]	GP_SIZE_MULT	General-purpose partition size	R/W	12	0x0
[142:140]	ENH_SIZE_MULT	Enhanced user data area size	R/W	3	0x0
[139:136]	ENH_START_ADDR	Enhanced user data start address	R/W	4	0x0
[135]	-	Reserved	TBD	1	-
[134]	SEC_BAD_BLK_MGMNT	Bad block management mode	R/W	1	0x0
[133]	PRODUCTION_STATE_AWARENES	Production state awareness	R/W/E	1	0x0
[132]	TCASE_SUPPORT	Package Case Temperature is controlled	W/E_P	1	0x0
[131]	PERIODIC_WAKEUP	Periodic wake up	R/W/E	1	0x0
[130]	PROGRAM_CID_CSD_DDR_SUPPORT	Program CID/CSD in DDR mode support	R	1	0x1
[129:128]	-	Reserved	TBD	2	-

ECSD Bytes	Field	Name	Cell Type1	Size (Bytes)	ECSD Value
[127:64]	VENDOR_SPECIFIC_FIELD	Vendor specific field	-	64	0x0
[63]	NATIVE_SECTOR_SIZE	Native sector size	R	1	0x0
[62]	USE_NATIVE_SECTOR	Sector size emulation	R/W	1	0x0
[61]	DATA_SECTOR_SIZE	Sector size	R	1	0x0
[60]	INI_TIMEOUT_EMU	1st initialization after disabling sector size emulation	R	1	0x0
[59]	CLASS_6_CTRL	Class 6 command control	R/W/E_P	1	0x0
[58]	DYNCAP_NEEDED	Number of addressed groups to be Released	R	1	0x0
[57:56]	EXCEPTION_EVENTS_CTRL	Exception events control	R/W/E_P	2	0x0
[55:54]	EXCEPTION_EVENTS_STATUS	Exception events status	R	2	0x0
[53:52]	EXT_PARTITIONS_ATTRIBUTE	Extended Partitions Attribute	R/W	2	0x0
[51:37]	CONTEXT_CONF	Context configuration	R/W/E_P	15	0x0
[36]	PACKED_COMMAND_STATUS	Packed command status	R	1	0x0
[35]	PACKED_FAILURE_INDEX	Packed command failure index	R	1	0x0
[34]	POWER_OFF_NOTIFICATION	Power Off Notification	R/W/E_P	1	0x0
[33]	CACHE_CTRL	Control to turn the Cache ON/OFF	R/W/E_P	1	0x0
[32]	FLUSH_CACHE	Flushing of the cache	W/E_P	1	0x0
[31]	BARRIER_CTRL	Control to turn the Barrier ON/OFF	R/W	1	0x0
[30]	MODE_CONFIG	Mode config	R/W/E_P	1	0x0
[29]	MODE_OPERATION_CODES	Mode operation codes	W/E_P	1	0x0
[28:27]	-	Reserved	TBD	2	0x0
[26]	FFU_STATUS	FFU status	R	1	0x0
[25:22]	PRE_LOADING_DATA_SIZE	Pre loading data size	R/W/E_P	4	0x0
[21:18]	MAX_PRE_LOADING_DATA_SIZE	Max pre loading data size	R	4	8GB: 0x00E90000 16GB: 0x009D8000 32GB: 0x01320000 64GB: 0x02760000 128GB: 0x04C98000 256GB: 0x09300000
[17]	PRODUCT_STATE_AWARENESS_ENABLEMENT	Product state awareness enablement	R/W/E&R	1	0x3
[16]	SECURE_REMOVAL_TYPE	Secure removal type	R/W&R	1	0x9
[15]	CMDQ_MODE_EN	Command Queue Mode Enable	R/W/E_P	1	0x0
[14:0]	-	Reserved	TBD	15	-

4.4.1 EXT_CSD_REV[192]

The protocol versions supported by the device are described in this register.

Table14: Protocol version

Timing Interface	Value	EXT_CSD Register Value
Reserved	255–9	0x08
Revision 1.8(for MMC V5.1)	8	
Revision 1.7(for MMC V5.0)	7	
Revision 1.6(for MMC V4.5，V4.51)	6	
Revision 1.5(for MMC V4.41)	5	
Revision 1.4(Obsolete)	4	
Revision 1.3(for MMC V4.3)	3	
Revision 1.2(for MMC V4.2)	2	
Revision 1.1(for MMC V4.1)	1	
Revision 1.0(for MMC V4.0)	0	

4.4.2 HS_TIMING[185]

Table15: Interface rate and drive strength

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
driver strength types				Timing interface rate			

This register is used by the host to select the timing interface rate and drive strength. This byte consists of two fields:

bit[3:0] : Timing interface rate, default 0 when powered on.

bit[7:4] : Drive strength types, default 0 when powered on.

Table16: Timing interface rate

Mode	Value	Remark
HS400 mode	0x3	200MHz DDR
HS200 mode	0x2	200MHz SDR
HS mode	0x1	52MHz SDR and DDR
Compatibility mode	0x0	26MHz SDR

Table17: I/O Drive strength types

Driver Type Values	Support	Nominal Impedance	Approximated driving capability compared to Type-0	Remark
0x0	Mandatory	50Ω	x1	Default Driver Type. Supports up to 200MHz operation.
0x1	Optional	33Ω	x1.5	Supports up to 200MHz operation.

Driver Type Values	Support	Nominal Impedance	Approximated driving capability compared to Type-0	Remark
0x2	Optional	66Ω	x0.75	The weakest driver that supports up to 200MHz operation.
0x3	Optional	100Ω	x0.5	For low noise and low EMI systems.Maximal operating frequency is decided by Host design.
0x4	Optional	40Ω	x1.2	

4.4.3 BUS_WIDTH[183]

Table18: Bus Width

Value	Bus Width
255–7	Reserved
6	DDR 8 bit data bus
5	DDR bit 4 data bus
4-3	Reserved
2	SDR 8 bit data bus
1	SDR 4bit data bus
0	SDR 1bit data bus

0 after power on (1-bit data bus), which can be changed with SWITCH command (CMD6). HS_TIMING must be set to 0x1 in order to set BUS_WIDTH to double data rate operation mode (0x5 or 0x6).

4.4.4 RST_n_FUNCTION[162]

Table19: Reset

bit7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved						RST_n_ENABLE	

bit[7:2] : Reserved;

bit[1:0) : RST_n_ENABLE (once to write);

0x0: RST_n signal temporary ban (default);

0x1: RST_n signal permanently enabled;

0x2: RST_n signal permanently forbidden;

0x3: Reserved.

For backward compatibility reasons, RST_n signal of devices that are temporary forbidden by default. The host can set this signal to be permanently enabled or permanently disabled before using the device.

General host Settings RST_n_ENABLE 0x2 (permanent ban), cannot accept RST_n signal input device will be permanently. During the ban, RST_n outside of any state (high, low, floating) not cause any problem with the device (such as the function is not normal and input cache large leakage current).

When RST_n_ENABLE is set to 0x1 (permanent enable), the device accepts input from RST_n permanently. The host is unable to change the bit back to the forbidden value. In addition, when the host sets RST_n_ENABLE to 0x1, the device must not trigger an internal circuit reset due to a register change. The internal reset sequence must be triggered by the rising edge of the external RST_n pin, not by a register change.

When not configured, because internal eMMC RST_n signal without any pull-up or pull-down resistor, the host must be up or down RST_n, lest the RST_n enabled when unnecessary leakage current to the input circuit operation.

4.5 RCA register

RCA is equipment relative address (RCA) registers, it is a 16-bit register, during the period of equipment to identify the host to the distribution of device address. This address for device identify routine after addressing the communication. The default value is 0x0001 of RCA register. The value 0x0000 is reserved for placing all devices in the Stand-by state with CMD7.

4.6 DSR register

DSR register is a device driver register, it is a 16-bit register, this is an optional register, can be used to extend the operating conditions in order to improve the bus performance (depending on the length of the bus, several parameters such as transmission rate or the number of the equipment).

5 eMMC partition

The initial eMMC partition is mainly divided into four parts: user data area, RPMB area and two boot areas.

Two Boot areas: This is where some system information, such as boot image and default configuration parameters, can be stored.

RPMB partitions: a RPMB partition can be accessed through credible mechanism, is used to deposit system of some special data, access authorization is required.

The User data area: users can directly access the region, the actual capacity for eMMC can see.

Figure4: eMMC Partition

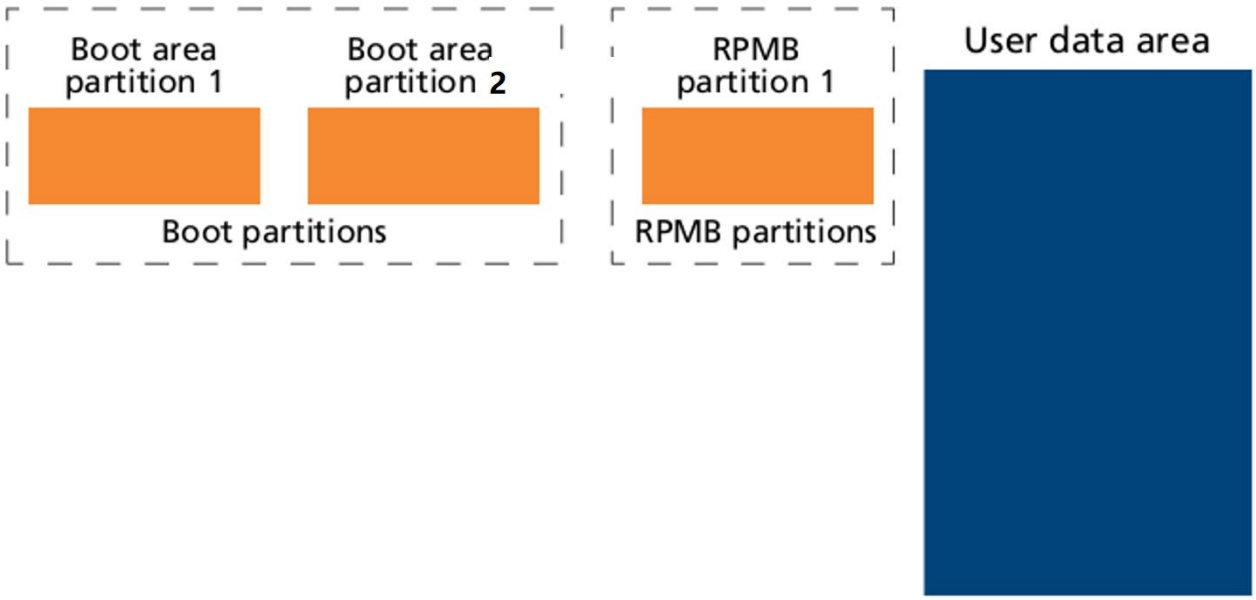


Table20: Boot and RPMB Size

	Boot 1 size	Boot2 size	RPMB size
Default	4096KB	4096KB	4096KB
Max	4096KB	4096KB	4096KB

6 Work mode

The five modes of operation of the eMMC: the Boot mode, the Card identification mode, the Interrupt mode, the Data transfer mode, the Inactive mode.

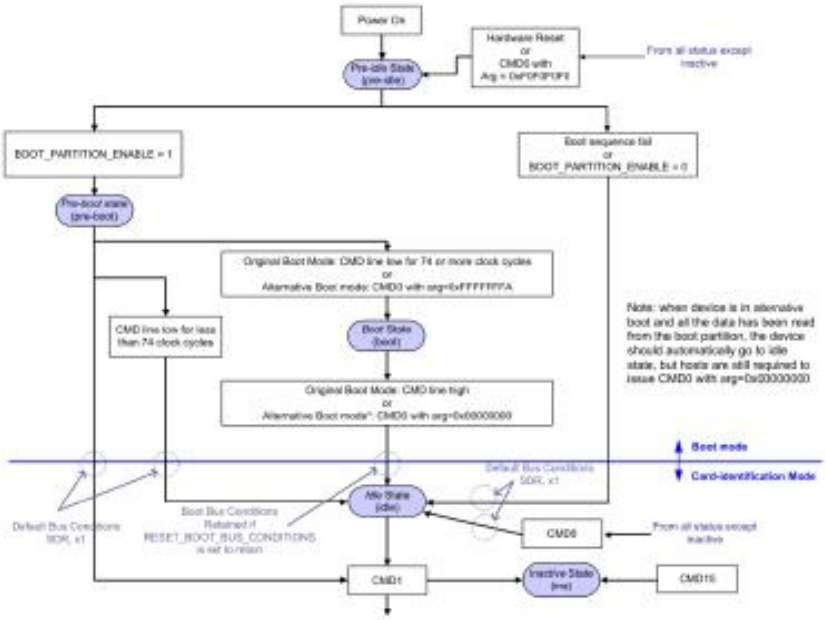
6.1 Boot mode

After Power ON, eMMC if receive CMD0 (GO_Idle_State) with parameters for "0xF0F0F0F0", if eMMC support at this time the Boot mode will enter the Boot mode, otherwise enter identification mode.

The Boot mode process is as follows:

- When the system power on, hardware reset or host a CMD0 instruction and with 0xF0F0F0F0, the system will enter the Pre-Idle State.
- Device will automatically detect whether BOOT_PARTITION_ENABLE is 1, if 0 is out of the Boot Mode, enter the Card-identification Mode. If is 1, enter the next step of the pre-boot state。

Figure5: Boot mode process



- The CMD line should be kept low for at least 74 clock cycles, or the host sends CMD0 with 0xFFFFFFFA, at which point the device will issue the data to be read by the host, and the host will receive it and jump to the Idle State in Card-identification Mode. Otherwise if the lower time less than 74 clock cycles, ends the Boot Mode and enter the Idle State in Card-identification Mode.

6.2 Card identification mode

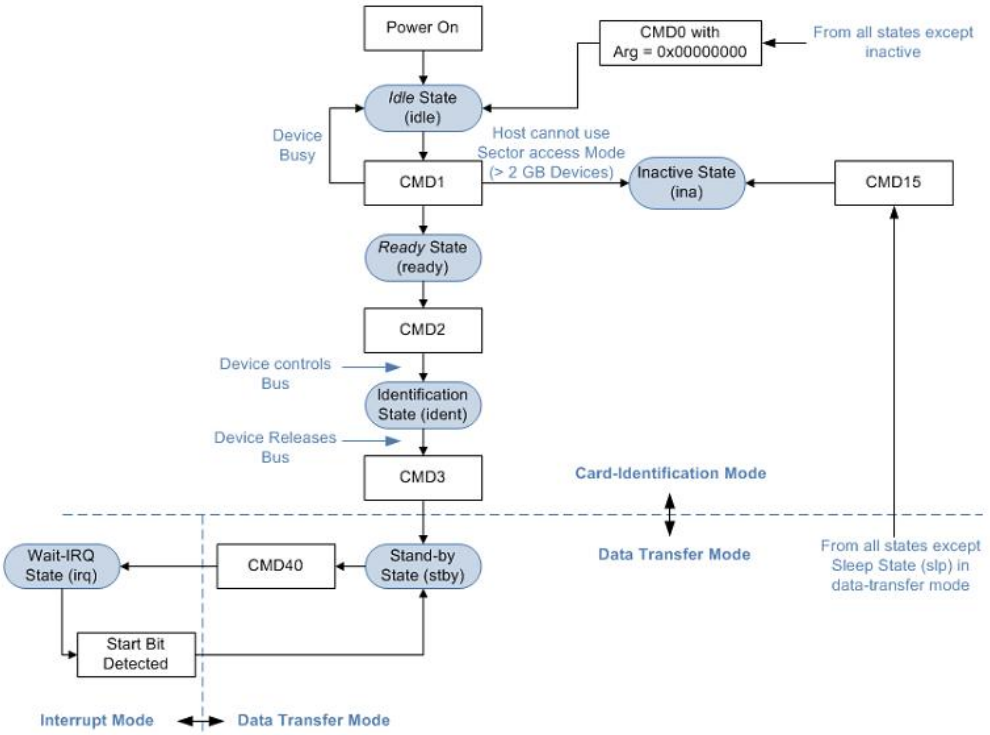
After Power ON, after the Boot mode to complete or does not support the Boot mode, the Card will enter under this pattern continue waiting for receiving Host CMD3 (Send_Relative_Address).

EMMC to work properly, must first complete the initialization process, in the process of initialization, the system will complete the recognition of eMMC, determine the equipment working voltage range and usage patterns, and assign device address (RCA, a system may have multiple eMMCs). This process is called the Card identification mode, all of the data communication in the process of initialization only on the CMD line. Device initialization flow chart is illustrated below:

The initialization process is as follows:

- The first step is enter the Idle State, there are two ways to enter the Idle State, one is through the Power On, the other is with 0x00000000 into CMD0 take parameters, CMD0 belong to a no response command.
- The second step is device into the Ready State, into the Ready State is done by CMD1, only send CMD1 with OCR format voltage parameter to MMC, receives the response voltage matching and the response of the highest bit busy bit is 1, is said equipment free to enter the Ready State. If received CMD1 voltage parameter mismatch, MMC, into the Inactive State, not any response to the subsequent process. If the Host IO voltage can be adjusted, need to read before the adjustment of OCR. In order not to make the equipment into the Inactive State, can send MMC CMD1 with no parameters, so that we can only get the OCR register, without changing the State of the equipment. In the process of identification, the Host can't change the voltage range, if need to be modified, the modified must restart the recognition process.

Figure6: Initialize the process



- In the Ready State, send CMD2 instruction, can make the eMMC into the Identification of the State. Send CMD2 if successful, the Host for CID register values, while the MMC into the Identification of the State. If you don't succeed, the device status remains the same. In the case of a single MMC Identification, as long as within the range, and on the right, should be able to accurately receive fODCID values, and into the Identification of the State.

- Afterwards the host sends CMD3 (SET_RELATIVE_ADDR) gives the device a relative device address (RCA), will be in the next step of data transmission mode (typically, the higher clock rate) addressing equipment.As receiving the RCA, equipment into the Stand-by mode, and the equipment is no longer the recognition of the next cycle to react. And equipment will be the output drive from leakage switch to push pull open.

6.3 Data transfer mode

When the eMMC received by Host for RCA, this equipment will enter the Data transfer mode, wait to read and write instructions. In this mode can be realized for eMMC programming, design of store attributes, read and write, erase, test of the bus, and so on. Is the core of eMMC mode. The Data transfer mode of the two common operations:

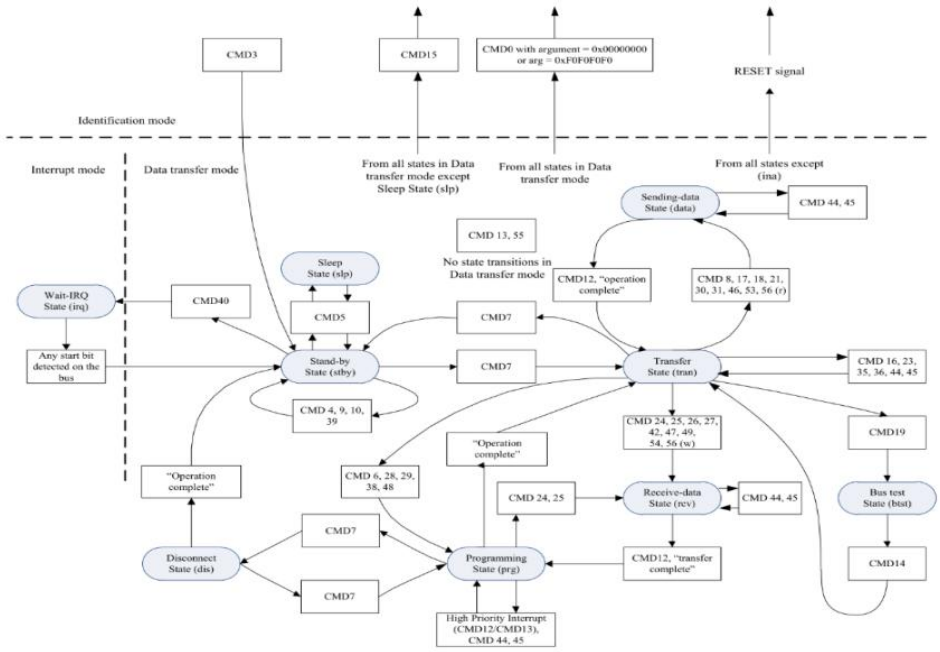
Read (single block and multiple block);

Write (single block and multiple block).

Read of single block:

- Equipment in Stand-by mode, the host sends CMD7 selected current device, the device will enter the transfer state mode;
- Send CMD16 SET_BLOCKLEN set to read block size, waiting for command response;
- Send CMD17 READ_SINGLE_BLOCK single block read command, waiting for the start of the command response to read data;
- Send a block size of data to complete read of single block.

Figure7: Data transfer mode process



Write of single block:

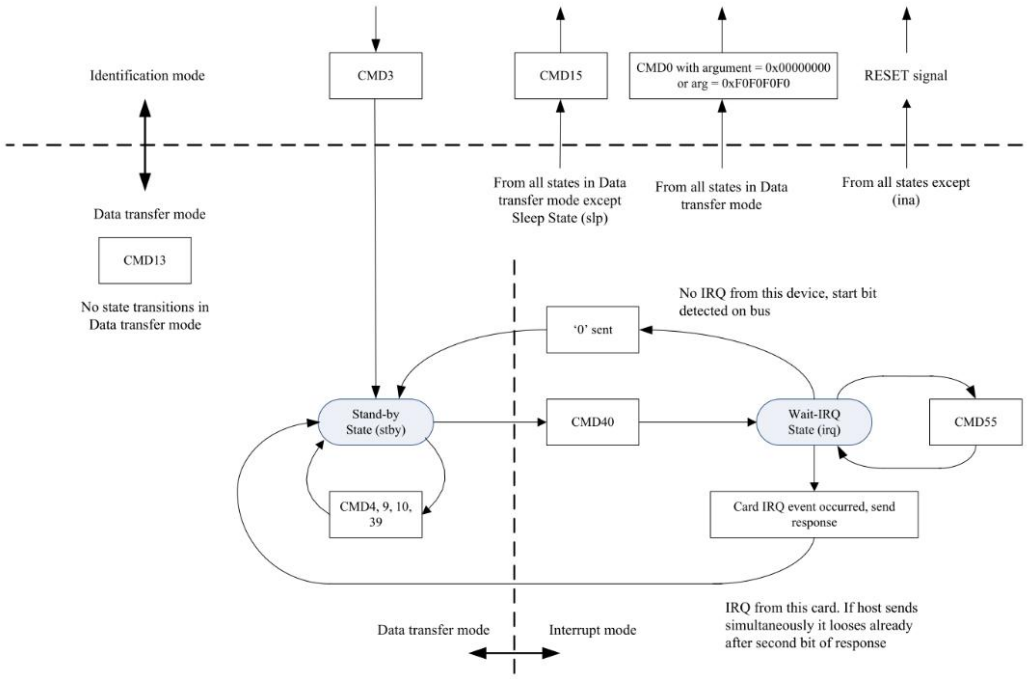
- Equipment in Stand by mode, the host sends CMD7 selected current device, the device will enter the transfer state state;
- Send CMD16 SET_BLOCKLEN set to read piece length, waiting for command response;
- Send CMD24WRITE_BLOCK single block write command;
- Send a block size of data to complete write of single block.

Other operations refer to JEDEC Standard No. 84 - B51 6.6.

6.4 Interrupt mode

Host and device will enter this mode at the same time, this mode will not do the Data Transfer, only allows the Host or Card sent interrupt service request.

Figure8: Interrupt mode



Interrupt mode related operations refer to JEDEC Standard No. 84 - B51 6.5.

6.5 Inactive mode

Card for voltage range or insert way will enter this mode when it is invalid, can also use CMD15 command to make a Card identified into the inactive state.

7 Electrical Parameter

7.1 Power range

Table21: Power range

Parameter	Description	Min	Typ	Max	Unit
V_{CC}	Supply voltage(NAND Flash)	2.7	3.3	3.6	V
V_{CCQ}	Supply voltage(Controller of NAND Flash and I/O)	2.7	3.3	3.6	V
		1.7	1.8	1.95	V
BUS LINE	All the data and control signals	-0.5	V_{CCQ}	V_{CCQ}+0.5	V

7.2 Bus load

Table22: Bus load

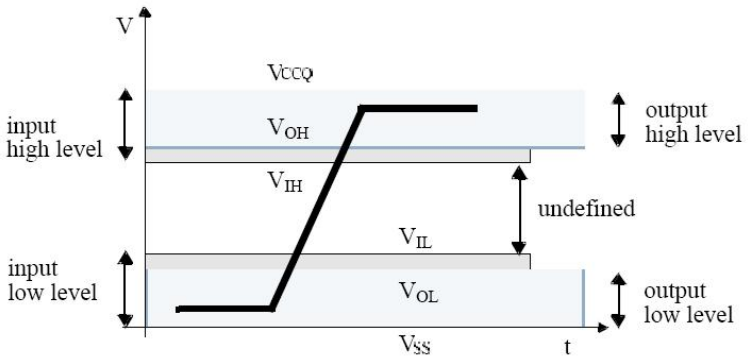
Parameter	Symbol	Min	Typ	Max	Unit	Description
CMD pull-up resistor	RCMD	4.7	--	100	kΩ	External pull up to V_{CCQ}
DAT0-7 pull-up resistor	RDAT	10	--	100	kΩ	External pull up to V_{CCQ}
DAT1-7 Internal pull-upresistor	Rint	10	--	150	kΩ	Prevent unconnectedlines from floating
Bus capacitance	C_L	--	--	30	pF	Single Device
Device capacitance	CDEVICE	--	--	12	pF	Single Device capacitance
Signal inductance	--	--	--	16	nH	fPP≤52MHz

eMMC bus for each line of the total capacitance (C_L) is the sum of the host capacitance (CHOST), bus capacitance itself (CBUS) and the eMMC connected to this line capacitance (CDEVICE): C_L=CHOST+CBUS+CDEVICE。

7.3 Bus level

Due to the power supply voltage is a variable value, all bus signal level related to the supply voltage.

Figure9: Bus level



7.3.1 Open-Drain Bus Signal Level

Table23: Open-Drain Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ}-0.2		V	Note
Output LOW voltage	V_{OL}		0.3	V	I_{OL}=2mA

Note: V_{OH} depends on external resistance value.

7.3.2 Bus signal level (high level)

The device input and output voltages shall be within the following specified ranges for any V_{CCQ} of the allowed voltage range.

V_{CCQ}（2.7V~3.6V）Push-pull signal level

Table24: V_{CCQ} push-pull signal level

Parameter	Symbol	Min	Max	Unit	Conditions (V_{CC}=3.3V)
Output HIGH voltage	V_{OH}	0.75*V_{CCQ}	--	V	I_{OH}=-100uA@V_{CCQ}=2.7V
Output LOW voltage	V_{OL}	--	0.125*V_{CCQ}	V	I_{OL}=100uA@V_{CCQ}=2.7V
Input HIGH voltage	V_{IH}	0.625*V_{CCQ}	V_{CCQ}+0.3	V	V_{CCQ}=3.3V
Input LOW voltage	V_{IL}	V_{SS}-0.3	0.25*V_{CCQ}	V	V_{CCQ}=3.3V

V_{CCQ}（1.7V~1.95V）push-pull signal level

Table25: V_{CCQ} push-pull signal level

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ}-0.45	--	V	I_{OH}=-2mA@V_{CCQ}=1.7V
Output LOW voltage	V_{OL}	--	0.45	V	I_{OL}=2mA@V_{CCQ}=1.7V
Input HIGH voltage	V_{IH}	0.65*V_{CCQ}	V_{CCQ}+0.3	V	V_{CCQ}=1.8V
Input LOW voltage	V_{IL}	V_{SS}-0.3	0.35*V_{CCQ}	V	V_{CCQ}=1.8V

7.4 Power-up sequence

Figure10: Power-up sequence

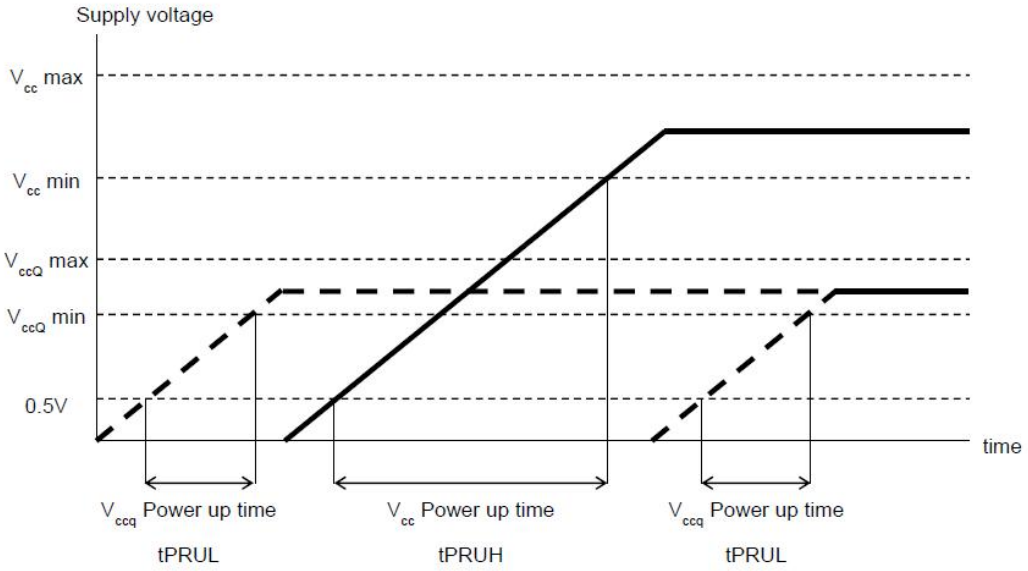


Table26: Power-up parameter

Parameter	Symbol	Min	Max	Remark
V_{CC}=3.3V	tPRUH	5μs	35ms	--
V_{CCQ}=1.8V	tPRUL	5μs	25ms	--

eMMC for power supply without order requirement, but the settling time of the power supply has the certain requirement, if it does not conform to the settling time of the power supply may cause unrecognized or accidental unrecognized.

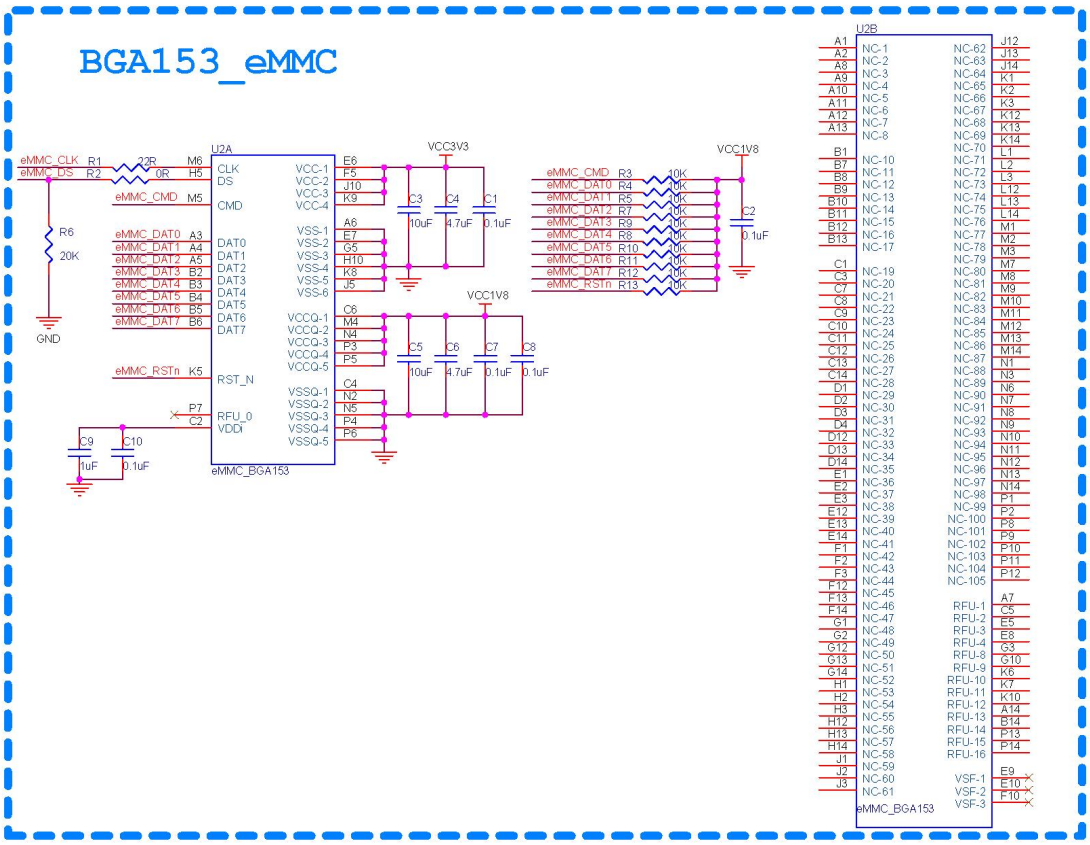
7.5 Recommend capacitance

Table27: Recommend capacitance

Parameter	Min	Typ	Max	Unit
V_{CC}	10		47	uF
V_{CCQ}	10		47	uF
VDDi	0.1		2.2	uF

8 Recommend design

Figure11: Recommend design (153ball)



Remark:

1. Filter capacitor should be as close as the V_{CC}/V_{CCQ} and V_{SS} pin.

2. The eMMC_IO for supply voltage according to the host for eMMC interface and actual usage pattern of user, but must keep consistent level with the host IO, disable level conversion chip, prevent level conversion chip is delayed, the read/write error of high-speed working mode.

3. Recommended layout GND between CLK, DS and DATA lines, DS, CMD, DAT0 ~ DAT7 line based on CLK around isometric arc line, single-ended impedance 50 ohm.

4. The unused IO disconnect with Host, the rest of use the resistors to pull-up, in consonance with the aforementioned referential schematic diagram.

9 Welding process

Chips must be bake for 9 hours before welding in atmosphere of 125℃(+10℃/-0℃) and less than 5% humidity.

According to the welding process to choose corresponding welding process parameters, temperature curve can refer to the figure below, reflow furnace temperature curve parameters for setting may refer to the table below. Furnace temperature curve setting should be combined with the parameters of the solder paste and other products on chip synthetically considered. Device encapsulating body reflow peak temperature is 260℃, the peak temperature of 250℃ to 260℃ for maximum 20s.

Figure12: Reflow soldering curve

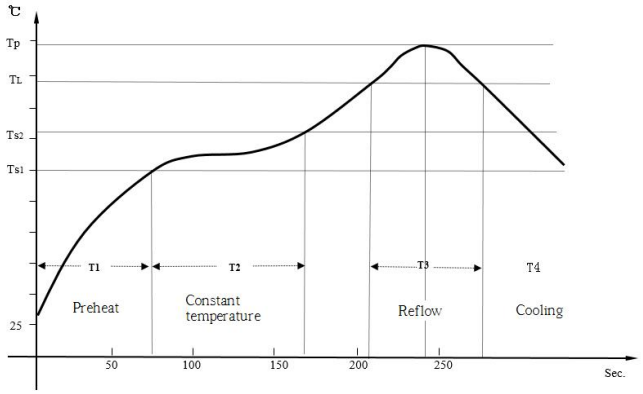


Table28: Reflow soldering process

Parameter of curve graph	Lead-free alloy
Liquidus temperature (TL)	220℃
Peak temperature range (Tp)	235℃-250℃
Minimum reflux peak temperature (Tp)	230℃
Heating slope (T1)	1.5℃/s-3℃/s
Cooling slope (T4)	2℃/s-5℃/s
Constant temperature zone temperature (T2)	150℃-180℃
Constant temperature zone time (T2)	60s-100s
Keep the time above liquidus(T3)	60s-90s

10 Other Notes

Chip for customized service is available, please contact to us if you need.

The datasheet is subject to upgrade without prior notice. If there is any difference between the datasheet and the product, please contact the manufacturer for the latest datasheet.